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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/750,093	12/29/2000	Michael Cornaby	2207/9806	6385

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KENYON & KENYON
Suite 700
1500 K Street, NW
Washington, DC 20005-1257

EXAMINER	
MEONSKE, TONIA L	
ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 03/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/750,093	CORNABY ET AL.	
	Examiner	Art Unit	
	Tonia L Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-10,13-15 and 18-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-10,13-15 and 18-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 4-10, 13-15, and 18-26 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Goss et al., US Patent 3,909,797.

3. Referring to claim 1, Goss et al. have taught a microinstruction sequencer including a microinstruction sequencer stack comprising an array of memory cells (Figure 2, element 60, including elements 62, 64, 66, and 68) microinstruction sequencing logic associated with the microinstruction sequencer stack, wherein the microinstruction sequencing logic determines if a microinstruction affects the microinstruction sequencer stack by determining if the microinstruction includes an operations encoding defined to control the microinstruction sequencer stack (Abstract, Figure 2, column 4, lines 48-64, column 6, column 7, line 64-column 8, line 62 When a microinstruction is a branch instruction, then the microinstruction will affect the microinstruction sequencer stack. Therefore, when the opcode of the microinstruction indicates a branch instruction, then the instruction is defined to control the microinstruction sequencer stack.).

4. Referring to claim 4, Goss et al. have taught the microinstruction sequencer of claim 1, as described above, and wherein the microinstruction sequencing logic includes logic to:

a. generate a value of a microinstruction address (Figure 2, Element 56 contains the generated microinstruction address.);

b. add an intermediary value to the value of the microinstruction address to yield an incremented value (Figure 2, element 58);

c. send a control value to the microinstruction sequencer stack, said control value to cause the incremented value to be pushed onto the microinstruction sequencer stack (Figure 2, The output of Element 58 is the control value that causes the incremented value to be pushed onto the stack.); and

d. push the incremented value onto the microinstruction sequencer stack (Abstract, Column 7, lines 60-64).

5. Referring to claim 5, Goss et al. have taught the microinstruction sequencer of claim 1, as described above, and wherein the microinstruction sequencing logic includes logic to:

a. send a control value to the microinstruction sequencer stack (Figure 2, Element 58 sends the control value to the stack.), said control value to:

i. cause the microinstruction sequencer stack to pop a value (abstract, column 8, lines 49-62); and

ii. send the popped value to a microinstruction address multiplexer (Figure 2, element 54).

6. Referring to claim 6, Goss et al. have taught the microinstruction sequencer of claim 1, as described above, and wherein the microinstruction sequencing logic includes logic to:

a. send a control value to the microinstruction sequencer stack, said control value to:

b. cause the microinstruction sequencer stack to pop a value (abstract, column 8, lines 49-62); and

c. send the popped value to an immediate logic (Figure 2, elements 54, 56, 50, and 52), said immediate logic to pass the value to a microprocessor core unit (Figure 2, Element 52 passes the value to the core unit.).

7. Referring to claim 7, Goss et al. have taught the microinstruction sequencer of claim 1, as described above, and wherein the microinstruction sequencing logic includes logic to send a control value to the microinstruction sequencer stack (Figure 2, Element 58 sends the control value to the stack.), said control value to cause the microinstruction sequencer stack to push a value in an immediate field of a microinstruction onto the microinstruction sequencer stack (Figure 2, The output of Element 58 is the control value that causes the incremented value to be pushed onto the stack.).

8. Referring to claim 8, Goss et al. have taught the microinstruction sequencer of claim 1, as described above, and wherein the microinstruction sequencing logic includes logic to send a control value to the microinstruction sequencer stack (Figure 2, Element 58 sends the control value to the stack.), said control value to cause the microinstruction sequencer stack to return to a reset state (Inherent, Must be able to initialize the system to a known state.).

9. Referring to claim 9, Goss et al. have taught the microinstruction sequencer of claim 1, wherein the microinstruction sequencing logic includes logic to send a control value to the microinstruction sequencer stack (Figure 2, Element 58 send control values to the stack.), said control value to cause the microinstruction sequencer stack to pop a value (abstract, column 8,

lines 49-62) and send the popped value to an immediate logic (Figure 2, elements 54, 56, 50, and 52).

10. Referring to claim 10, Goss et al. have taught the microinstruction sequencer of claim 1, as described above, and wherein the microinstruction sequencing logic includes logic to send a control value to the microinstruction sequencer stack (Figure 2, Element 58 sends the control value to the stack.), said control value to cause the microinstruction sequencer stack to send a value at the top of the microinstruction sequencer stack to an immediate logic (abstract, column 8, lines 49-62, Figure 2, elements 54, 56, 50, and 52).

11. Referring to claim 13, Goss et al. have taught a microprocessor including a microinstruction sequencer comprising:

a. an array of memory cells dedicated to a microinstruction sequencer stack (Figure 2, elements 62, 64, 66, and 68);

b. an address multiplexer coupled to the array of memory cells (Figure 2, element 54);

c. sequencing logic coupled to the address multiplexer and to the array of memory cells (Figure 2, elements 56, 50, 52, and 58),

d. wherein the sequencing logic determines if a microinstruction affects the microinstruction sequencer stack by determining if the microinstruction includes an operations encoding defined to control the microinstruction sequencer stack (Abstract, Figure 2, column 4, lines 48-64, column 6, column 7, line 64-column 8, line 62 When a microinstruction is a branch instruction, then the microinstruction will affect the microinstruction sequencer stack. Therefore, when the opcode encoded in the

microinstruction indicates a branch instruction, then the instruction is defined to control the microinstruction sequencer stack.); and

e. a microprocessor core unit coupled to the array of memory cells (The entire system in Figure 1 is a microprocessor core unit.).

12. Referring to claim 14, Goss et al. have taught the microinstruction sequencer of claim 13, wherein the microprocessor core unit is an execution unit (Figure 1).

13. Referring to claim 15, Goss et al. have taught the microinstruction sequencer of claim 13, as described above, and wherein the microprocessor core unit is a retire unit (Abstract, column 2, lines 39-44, In order for the instructions in the subroutine to be completed, there must inherently be unit that performs the completing.).

14. Claim 18 does not recite limitations above the claimed invention set forth in claim 1 and is therefore rejected for the same reasons set forth in the rejection of claim 1 above.

15. Claim 19 does not recite limitations above the claimed invention set forth in claim 13 and is therefore rejected for the same reasons set forth in the rejection of claim 13 above.

16. Claim 20 does not recite limitations above the claimed invention set forth in claim 4 and is therefore rejected for the same reasons set forth in the rejection of claim 4 above.

17. Claim 21 does not recite limitations above the claimed invention set forth in claim 5 and is therefore rejected for the same reasons set forth in the rejection of claim 5 above.

18. Claim 22 does not recite limitations above the claimed invention set forth in claim 6 and is therefore rejected for the same reasons set forth in the rejection of claim 6 above.

19. Claim 23 does not recite limitations above the claimed invention set forth in claim 7 and is therefore rejected for the same reasons set forth in the rejection of claim 7 above.

20. Claim 24 does not recite limitations above the claimed invention set forth in claim 8 and is therefore rejected for the same reasons set forth in the rejection of claim 8 above.

21. Claim 25 does not recite limitations above the claimed invention set forth in claim 9 and is therefore rejected for the same reasons set forth in the rejection of claim 9 above.

22. Claim 26 does not recite limitations above the claimed invention set forth in claim 10 and is therefore rejected for the same reasons set forth in the rejection of claim 10 above.

23. Claim 27 does not recite limitations above the claimed invention set forth in claim 14 and is therefore rejected for the same reasons set forth in the rejection of claim 14 above.

24. Claim 28 does not recite limitations above the claimed invention set forth in claim 15 and is therefore rejected for the same reasons set forth in the rejection of claim 15 above.

Conclusion

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, 8-4:30.

26. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

27. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100